to a first bus, and said at least one output terminal is coupled to a second bus, and each of the first and second buses is a unidirectional bus for transferring a signal or data in one direction.

4. (Amended) A semiconductor memory device comprising:

a plurality of input terminals for receiving write data, a control signal and an address signal;

at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting read data,

a write conversion circuit coupled between an internal data bus and the input terminal(s) for converting write data applied to said input terminal(s) into internal write data being equal in bit width to said internal data bus, and outputting said internal write data; and

a read conversion circuit coupled between said internal data bus and the output terminal for converting internal read data read onto said internal data bus into data being equal in bit width to said at least one output terminal, and transferring converted data to said at least one output terminal.

15. (Amended) The semiconductor memory device according to claim 3, wherein the input terminals receive the write data, the control signal and the address signal at common terminals.